

HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
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(0-30-00)

PATENT APPLICATION

ATTORNEY DOCKET NO. 10981967-1

JC944 U.S. PRO  
JC09/699080  
10/26/00

A



IN THE  
U.S. PATENT AND TRADEMARK OFFICE

10/26/00

Anticipated Classification of this application:

Class \_\_\_\_\_ Subclass \_\_\_\_\_

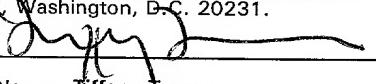
Prior application:

Examiner: Wille, D  
Art Unit: 2814

"Express Mail" label no.: EL188088047US

Date of Deposit: 10/26/00

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

By 

Typed Name: Tiffany Turner

ASSISTANT COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

**REQUEST FOR A CONTINUING APPLICATION UNDER 37 CFR 1.53(b)**

Sir:

This is a request for filing a continuing application under 37 CFR 1.53(b) a  
( ) continuation application of:  
(X) divisional application of:

**Pending Prior Application**

Application Serial No. 09/280,188 filed 3/29/99 .

Title Molecular Wire Transistors (MWT)

Name of applicant(s) Philip J. Kuekes, et al

**Copy of Application**

- (X) Enclosed is a copy of the prior application, including the drawings.  
( ) Enclosed is a new specification, including new drawings.

**Oath or Declaration**

- (X) Enclosed is a copy of the prior Declaration (37 CFR 1.63(d)).  
( ) Enclosed is a newly executed Declaration (original or copy).

**Foreign Priority - 35 USC 119**

- ( ) Foreign priority under 35 U.S.C. 119 has been claimed in prior application Serial No. \_\_\_\_\_  
filed on \_\_\_\_\_ in \_\_\_\_\_  
( ) The certified copy has been filed in prior application Serial No. \_\_\_\_\_  
filed \_\_\_\_\_  
( ) A separate paper claiming direct priority to a foreign application is enclosed herewith. A certified copy  
of the foreign application will be provided in due course.

**Relate Back - 35 USC 120**

- (X) Amend the specification after the title by inserting the following heading:

--Cross Reference To Related Application(s)--;

and add the paragraph:

--This is a ( ) continuation (X) divisional  
of copending application serial number 09/280,188 filed on 3/29/99 .

Inventorship Statement

- ( ) Delete the following named individuals as inventors in this application in accordance with 37 CFR 1.53(b) as a result of a change in the claimed subject matter:

Appointment of Associate Attorney

- ( ) Recognize as Associate Attorney or Agent \_\_\_\_\_

Registration No. \_\_\_\_\_

( ) authorization is hereby granted by signature below of the Attorney or Agent of record

( ) the Associate Attorney or Agent shall not have the authority to appoint other Attorneys or Agents

Communications

- (X) Address all future communications to: Direct telephone calls to:

HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P. O. Box 272400  
Fort Collins, Colorado 80528-9599

Marc. P. Schuyler  
(650) 857-3359

Other Amendments

- (X) Before calculating the filing fee, amend the prior application as follows:

(X) Cancel the following claims 1-15, 31-46 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes).

- (X) Enter the enclosed Preliminary Amendment.

Fee Calculation

- (X) The filing fee is calculated below for (X) Utility ( ) Design

| CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY     |                     |                     |             |               |
|--|---------------------|---------------------|-------------|---------------|
| (1)<br>FOR                                       | (2)<br>NUMBER FILED | (3)<br>NUMBER EXTRA | (4)<br>RATE | (5)<br>TOTALS |
| TOTAL CLAIMS                                     | 15 — 20             | 0                   | X \$18      | \$ 0          |
| INDEPENDENT CLAIMS                               | 3 — 3               | 0                   | X \$78      | \$ 0          |
| ANY MULTIPLE DEPENDENT CLAIMS                    | 0                   |                     | \$260       | \$ 0          |
| BASIC FEE: Design \$310.00 ); Utility \$690.00 ) |                     |                     |             | \$ 690        |
| TOTAL FILING FEE                                 |                     |                     |             | \$ 690        |
| TOTAL CHARGES TO DEPOSIT ACCOUNT                 |                     |                     |             | \$ 690        |

Charge \$ 690 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,

Philip J. Kuekes

By

Marc P. Schuyler

Attorney/Agent for Applicant(s)  
Reg. No. 35,675

Date: 10/26/00

Telephone No.: (650) 857-3359

IN THE PATENT AND TRADEMARK OFFICE

|   |   |                  |
|---|---|------------------|
| In re divisional patent application of: | ) | Group Art Unit:  |
| KUEKES ET AL.                           | ) | 2814             |
|   | ) |                  |
| For: MOLECULAR WIRE TRANSISTORS (MWT)   | ) | Examiner:        |
|   | ) | Willie, D.       |
| Prior Application Filing Date:          | ) |                  |
| 29 March 1999                           | ) | Attorney Docket: |
|   | ) | 10981967-1       |
| Prior Application Number:               | ) |                  |
| 09/280,188                              | ) | Palo Alto, CA    |
|   | ) | 25 October 2000  |

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PRELIMINARY AMENDMENT

Commissioner of Patents and Trademarks  
Assistant Commissioner for Patents  
Washington, DC 20231

Sir:

Prior to examination, please enter this preliminary amendment in connection with a divisional patent application directed toward claims 16-30.

In The Specification.

Page 1, line 11, please change " \_\_\_\_\_ " to read --09/280,225--.

Page 1, line 12, please delete "[PD-10981966-1]", change " \_\_\_\_\_ " to read --09/280,189--, and delete "[PD".

Page 1, line 13, please delete "10981968-1]", change " \_\_\_\_\_ " to read --09/280,045--, and delete "[PD-10981969-1]".

Page 1, line 14, please change " \_\_\_\_\_ " to read --09/280,049--, and delete "[PD-10981970-1]".

Page 1, line 15, please change "; \_\_\_\_\_" to read --09/280,048--.

Page 1, line 16, please delete "[10981971-1]".

Page 1, bridging lines 17-18, please delete "\_\_\_\_\_ [PD-10981971-1]" and insert in place thereof --09/280,048--.

Page 1, bridging lines 18-19, please delete "\_\_\_\_\_ [PD-10981969-1]" and insert in place thereof --09/280,045--.

Page 1, bridging lines 19-20, please delete "\_\_\_\_\_ [PD-10981966-1]" and insert in place thereof --09/280,225--.

Page 3, line 2, please change "\_\_\_\_\_ " to read --09/280,048-- and delete "[PD-10981971-1]".

Page 7, line 23, please change "\_\_\_\_\_ " to read --09/280,048--.

Page 7, bridging lines 23-24, please delete "[PD-10981971-1]".

Page 15, line 5, please change "\_\_\_\_\_ " to read --09/280,048--.

Page 15, line 6, please delete "[PD-10981971-1]".

### In the Claims.

Please cancel claims 1-15 and 31-46, without prejudice.

27. (Once Amended) The method of Claim 16 wherein said second wire also comprises a semiconductor material, and wherein both said semiconductor wires are provided with functional

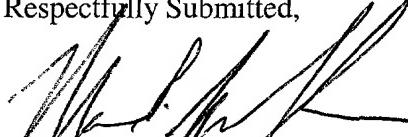
groups, one said wire being provided with Lewis acid functional groups and the other said wire being provided with Lewis base functional groups.

### REMARKS

In connection with the parent application referenced in the header of this paper, there was confusion over which set of claims Applicants elected, with Applicants contending that the wrong set of claims was being examined. Rather than perpetuate this confusion via a file wrapper continuation, Applicants have elected to "clear the air" and pursue each set of claims via separate divisional patent applications.

Applicants note that the last office action in the parent case examined claims 16-30. To put the present application in the same condition as the parent case, Applicants will be filing two preliminary responses. The first response, effected by this paper, is a preliminary amendment made to conform the form present application to the parent. The second response will be made by outside counsel as a substantive response to the most recent office action in the parent case.

Respectfully Submitted,



Marc P. Schuyler  
Registration No. 35,675

"Express Mail" mailing label number EL 187266510 US

Date of Deposit March 29, 1999

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" services under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

PATENT

PD-10981967-1

Typed Name of Person Mailing Paper or Fee Linda A. Iimura

Signature Linda A. Iimura

## MOLECULAR WIRE TRANSISTOR (MWT)

### INVENTORS:

Philip J. Kuekes

R. Stanley Williams

PATENT  
PD-10981967-1

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## MOLECULAR WIRE TRANSISTOR (MWT)

### CROSS-REFERENCE TO RELATED APPLICATIONS

10        The present application is related to the following applications: Serial Numbers \_\_\_\_\_ (“Molecular Wire Crossbar Interconnects for Signal Routing and Communications”) [PD-10981966-1]; \_\_\_\_\_ (“Molecular Wire Crossbar Memory”) [PD-10981968-1]; \_\_\_\_\_ (“Molecular Wire Crossbar Logic”) [PD-10981969-1];  
15        \_\_\_\_\_ (“Demultiplexer for a Molecular Wire Crossbar Network”) [PD-10981970-1];  
and \_\_\_\_\_ (“Chemically Synthesized and Assembled Electronic Devices”) [PD-10981971-1], all filed on even date herewith. The present application employs the chemical synthesis and assembly techniques disclosed and claimed in \_\_\_\_\_ [PD-10981971-1] and is used in the demultiplexer disclosed and claimed in \_\_\_\_\_ [PD-10981969-1] and the crossbar interconnections disclosed and claimed in \_\_\_\_\_ [PD-20        10981966-1].

### TECHNICAL FIELD

25        The present invention relates generally to electronic devices whose functional length scales are measured in nanometers, and, more particularly, to transistors based on crossed nanometer-scale wires, at least one of which is a modulation-doped semiconductor, joined by functionalized groups at the intersecting junctions.

BACKGROUND ART

The silicon (Si) integrated circuit (IC) has dominated electronics and has helped it grow to become one of the world's largest and most critical industries over  
5 the past thirty-five years. However, because of a combination of physical and economic reasons, the miniaturization that has accompanied the growth of Si ICs is reaching its limit. The present scale of devices is on the order of tenths of micrometers. New solutions are being proposed to take electronics to ever smaller levels; such current solutions are directed to constructing nanometer scale devices.

10 Prior proposed solutions to the problem of constructing nanometer scale devices have involved (1) the utilization of extremely fine scale lithography using X-rays, electrons, ions, scanning probes, or stamping to define the device components; (2) direct writing of the device components by electrons, ions, or scanning probes; or (3) the direct chemical synthesis and linking of components with covalent bonds. The  
15 major problem with (1) is that the wafer on which the devices are built must be aligned to within a small fraction of the size of the device features in at least two dimensions for several successive stages of lithography, followed by etching or deposition to build the devices. This level of control does not scale well as device sizes are reduced to nanometer scale dimensions. It becomes extremely expensive to implement  
20 as devices are scaled down to nanometer scale dimensions. The major problem with (2) is that it is a serial process, and direct writing a wafer full of complex devices, each containing trillions of components, could well require many years. Finally, the problem with (3) is that high information content molecules are typically macromolecular structures such as proteins and DNA, and both have extremely complex and, to date, unpredictable secondary and tertiary structures that cause them to twist into helices, fold into sheets, and form other complex 3D structures that will have a significant and usually deleterious effect on their desired electrical properties as well as make interfacing them to the outside world impossible.  
25

30 The present inventors have developed new approaches to nanometer-scale devices, comprising crossed nano-scale wires that are joined at their intersecting junc-

tions with bi-stable molecules, as disclosed and claimed in application Serial No. \_\_\_\_\_, filed on even date herewith [PD-10981971-1]. Wires, such as silicon, carbon and/or metal, are formed in two-dimensional arrays. A bi-stable molecule, such as rotaxane or pseudo-rotaxane, is formed at each intersection of a pair of wires. The bi-stable molecule is switchable between two states upon application of a voltage along a selected pair of wires.

Prior solutions to the problem of constructing a nanometer scale transistor (a three-terminal device with gain) involve the precise positioning of three or four components within a nanometer. A proposed prior solution is to position a quantum dot between two wires, which act as the source and drain of the transistor, in tunneling contact with the quantum dot (this is known as a single-electron transistor, or SET, and was originally proposed by K. Likharev); see, e.g., K.K. Likharev, "Correlated discrete transfer of single electrons in ultrasmall tunnel junctions", IBM Journal of Research and Development, Vol. 32, pp. 144-158 (January 1998). A third wire is positioned in capacitive contact with the dot, which is the gate. The voltage on the gate changes the energy levels in the quantum dot, which creates a coulomb blockade to current flowing from the source to the drain.

The problem with the foregoing construction is that a total of three wires plus a quantum dot have to be precisely positioned. This precision of placement must clearly be better than the sizes of the components being placed, which are in the order of nanometers. Such devices have been fabricated using conventional lithography, in which case they are so large they must be operated at very low temperatures (near absolute zero). They have also been fabricated using electron beam lithography and utilizing scanning probe microscopes as direct-write tools.

Thus, there remains a need to provide a nanoscale transistor that affords the advantages of prior art devices, while avoiding most, if not all, their disadvantages.

DISCLOSURE OF INVENTION

In accordance with the present invention, a molecular wire transistor is provided, comprising a pair of crossed wires, with at least one of the wires comprising a modulation-doped semiconductor material. A first semiconductor wire is of a first conductivity type and a second wire is provided with either Lewis acid functional groups or Lewis base functional groups to create a region of modulation doping of a second and opposite conductivity type in the junction.

If both functionalized wires are doped semiconductor, such as silicon, one is P-doped and the other is N-doped. One wire of a given doping comprises the "emitter" and "collector" portions and the other wire induces the "base" function in the first wire containing the emitter and collector at the junction where the wires cross, between the emitter and collector portions. The "base" region is always modulation-doped in the present invention. Both PNP and NPN transistors that are analogous to bipolar transistors may be formed in this fashion.

One functionalized wire may comprise doped semiconductor, such as silicon, and the other functionalized wire may comprise a metal. Here, the doped semiconductor wire comprises the "source" and "drain" and the metal wire induces the "gate" function on the doped semiconductor wire where the wires cross, between the source and drain, to form a field effect transistor. The "gate" region is always modulation-doped in the present invention. Both N-channel and P-channel transistors that are analogous to field effect transistors may be formed in this fashion.

Further, a molecular memory effect (state change) may be incorporated into the coatings that dope the wires. By choosing the molecule that does the doping of the gate to have two distinct oxidation-reduction (redox) states, a conductive state and a relatively insulating state with a large I-V hysteresis separating the two, it then becomes possible to have a special type of transistor. If the state change is set, then a transistor is formed, but if the state change is not set, then either an open or closed switch is formed. Whether a switch is open or closed depends on the state of a wire coating - whether it is oxidize or reduced.

A second version of molecular memory effect (molecular configuration bit) is to use a bi-stable molecule such that if the memory bit is set, the semiconductor wire is N-doped along its entire length and conducts. But if the memory bit is reset by applying a sufficient voltage difference between the two wires, then the molecule induces a P region through modulation doping, and the semiconductor wire will not conduct across the region where the wires cross. The N and P regions can be interchanged to make another form of the invention.

The present invention enables the construction of transistors on a nanometer scale, which are self-aligned and modulation-doped. It is very difficult at a nanometer scale to position and align the three components of a bipolar transistor (emitter, base 10 collector) or a field effect transistor (source, gate, and drain). It is also very difficult at a length scale defined in angstroms to control the exact properties of the doping that defines the electrical properties of the semiconductor.

The present invention allows transistors to be formed with a size on the order 15 of tens of nanometers to a few nanometers. By choosing the molecules which form the doping layer, it is possible to build transistors with a wide variety of specifically desired electrical properties. The inclusion of an electrically settable memory bit, through an electrochemical reaction with a large hysteresis loop in its I-V characteristic, as part of the molecules that define the gate region allows a new and useful function 20 to be added to transistors. Another advantage of this invention is that the same technology allows one to choose to build both NPN and PNP bipolar transistors as well as P-channel and N-channel FETs.

#### BRIEF DESCRIPTION OF THE DRAWINGS

25

FIG. 1A is a schematic representation of two crossed nano-scale wires, with at least one molecule bridging the gap in accordance with the invention;

FIG. 1B is a perspective view, depicting the device shown in FIG. 1A;

FIG. 2 is a schematic representation of two crossed nanowires, joined by a rotaxane, and depicting the two bi-stable states;

FIG. 3 is a representation similar to that shown in FIG. 1A, depicting a diode formed by two crossed nano-scale wires;

FIG. 4 is a representation similar to that of FIG. 1B, but showing two separate wires having modulation doping from external molecular coatings, prior to forming a  
5 transistor;

FIG. 5 is a representation similar to that of FIG. 4, where both wires are doped semiconductors, but showing the formation of a molecular wire bipolar transistor, here, NPN (collector-base-emitter);

10 FIG. 6 is a representation similar to that of FIG. 5, where one wire is doped semiconductor and the other wire is metal, showing the formation of a molecular wire field effect transistor, here, P-channel; and

FIG. 7 is a schematic diagram depicting a crossbar interconnect and showing the features that enable construction of an arbitrarily complex integrated circuit.

15 **BEST MODES FOR CARRYING OUT THE INVENTION**

**Definitions**

As used herein, the term “self-aligned” as applied to “junction” means that the junction that forms the switch and/or other electrical connection between two wires is created wherever two wires, either of which may be coated or functionalized, cross each other, because it is the act of crossing that creates the junction.  
20

The term “self-assembled” as used herein refers to a system that naturally adopts some geometric pattern because of the identity of the components of the system; the system achieves at least a local minimum in its energy by adopting this configuration.  
25

The term “singly configurable” means that a switch can change its state only once via an irreversible process such as an oxidation or reduction reaction; such a switch can be the basis of a programmable read only memory (PROM), for example.

The term “reconfigurable” means that a switch can change its state multiple times via a reversible process such as an oxidation or reduction; in other words, the  
30

switch can be opened and closed multiple times such as the memory bits in a random access memory (RAM).

The term "bi-stable" as applied to a molecule means a molecule having two relatively low energy states. The molecule may be either irreversibly switched from 5 one state to the other (singly configurable) or reversibly switched from one state to the other (reconfigurable).

Micron-scale dimensions refers to dimensions that range from 1 micrometer to a few micrometers in size.

Sub-micron scale dimensions refers to dimensions that range from 1 10 micrometer down to 0.04 micrometers.

Nanometer scale dimensions refers to dimensions that range from 0.1 nanometers to 50 nanometers (0.05 micrometers).

Micron-scale and submicron-scale wires refers to rod or ribbon-shaped conductors or semiconductors with widths or diameters having the dimensions of 1 to 10 15 micrometers, heights that can range from a few tens of nanometers to a micrometer, and lengths of several micrometers and longer.

A crossbar is an array of switches that connect each wire in one set of parallel wires to every member of a second set of parallel wires that intersects the first set (usually the two sets of wires are perpendicular to each other, but this is not a necessary condition). 20

#### Crossed Wire Switch

In related patent application Serial No. \_\_\_\_\_, filed on even date herewith [PD-10981971-1], a basic scheme for chemically synthesized and assembled electronic devices is provided. That application discloses and claims a quantum state switch, which 25 comprises an adjustable tunnel junction between two nanometer-scale wires. In accordance with that invention, an electronic device is provided, comprising two crossed wires having nanometer dimensions, provided with functionalizing groups that control conductivity type of the wires. A plurality of such crossed wires may be assembled to 30 provide a variety of different devices and circuits.

That invention enables the construction of electronic devices on a nanometer scale using relatively stiff wires that are chemically functionalized to provide the desired electronic properties and which are then chemically-assembled to create active electronic devices simply by forming contact with other wires.

The essential device features are shown in FIGS. 1A-1B. A crossed wire switch 10 comprises two wires 12, 14, each either a metal or semiconductor wire, that are crossed at some non-zero angle. In between those wires is a layer of molecules or molecular compounds 16, denoted R in FIGS. 1A and 1B. The particular molecules 18 (denoted  $R_s$ ) that are sandwiched at the intersection, or junction, of the two wires 12, 14 are identified as switch molecules. When an appropriate voltage is applied across the wires, the switch molecules are either oxidized or reduced. When a molecule is oxidized (reduced), then a second species is reduced (oxidized) so that charge is balanced. These two species are then called a redox pair. One example of this device would be for one molecule to be reduced, and then a second molecule (the other half of the redox pair) is oxidized. In another example, a molecule is reduced, and one of the wires is oxidized. In a third example, a molecule is oxidized, and one of the wires is reduced. In a fourth example, one wire is oxidized, and an oxide associated with the other wire is reduced. In all cases, oxidation or reduction will affect the tunneling distance or the tunneling barrier height between the two wires, thereby exponentially altering the rate of charge transport across the wire junction, and serving as the basis for a switch.

Further, FIG. 1B depicts a coating 20 on wire 12 and a coating 22 on wire 14. The coatings 20, 22 may be modulation-doping coatings, tunneling barriers (e.g., oxides), or other nano-scale functionally suitable materials. Alternatively, the wires 12, 14 themselves may be coated with one or more R species 16, and where the wires cross,  $R_s$  18 is formed.

That invention allows electronic devices to be formed with a size on the order of tens of nanometers to a few nanometers simply by making contact between two wires. By choosing the molecules which form a doping layer on the wires (modulation doping), it is possible to build devices with a wide variety of specifically desired

electrical properties. The possibility of reversibly or even irreversibly changing the properties of the device via an electrochemical reaction with a large hysteresis loop in its I-V characteristic enables devices to be altered after they are built and may provide new and useful functions.

5       The electronic device 10 of that invention, in its simplest state, is a quantum state switch comprising an adjustable tunnel junction 18 between two nanometer-scale wires 12, 14. A plurality of sets of wires, one set configured at an angle to the other, provides a two-dimensional array of switches. The wires are provided with a molecular species 16 at the junctions 18 that, in one embodiment, is bi-stable. The molecule species is addressed by setting voltages on the appropriate two wires. Thus, by the simple process of crossing one type of coated wire over the other, a switch is formed at wherever the intersection occurs; the exact position of the connecting point is not important for this architecture. Furthermore, the chemical species that form the molecular link between the wires can be electrochemically oxidized or reduced. Some types of molecules can be cycled reversibly and others will react irreversibly. The chemical state of the molecular switches determines the tunneling resistance between the two wires, which is exponentially dependent on both the width and the barrier height of the tunneling gap.

20      An example of a bi-stable molecular switch 110 is shown in FIG. 2, comprising a rotaxane 24. The rotaxane 24 contains two molecular components - a backbone 24a that contains one or more binding sites, and a circular molecule (the 'ring') 24b that fits around the backbone like a ring on a post. The ring 24b is in intimate mechanical contact, but is not chemically bonded to the backbone 24a. Depending on how the ring is fabricated, the ring may have one or more preferred minimum-energy locations along 25 the backbone. In FIG. 2, these sites are denoted 26 (left site) and 28 (right site).

The moiety 29 on the left side of the rotaxane 24 shows that the molecule is asymmetric and therefore can have different properties when oxidized than when reduced.

Molecular Wire TransistorA. Diodes

Essential to the fabrication of transistors, first, the fabrication of diodes employing the teachings of the present invention must be understood.

FIG. 3 shows the intersection of two wires 12, 14 that have been separately doped, one to be a P-type semiconductor, the other to be an N-type semiconductor. The wires 12, 14 are manufactured by the same process, and then doped separately to form the two wire types. After forming the doped wires, they are brought together to form a diode 30. This is very different from existing integrated circuit processes that make and dope the semiconductor components in the place where they are to be used. The diode shown in FIG. 3 is a self-assembling device that has the design parametric advantages that lithographically-formed devices have: the engineer designing the circuits can control the dimensions and the strength of the doping and thus the electrical properties.

15

B. "Bipolar" Transistors

The intrinsic difficulty in constructing a transistor at a nanometer size is that three components have to be brought together with a precise geometric relationship. The bipolar molecular wire transistor (MWT) of the present invention is constructed simply by crossing two differently doped semiconductor molecular wires together at a point. The point can be anywhere along either wire; the topological fact that the wires intersect creates the bipolar transistor. Wherever the point of intersection is, a transistor will be formed. The four ends of the two wires are the electrical contacts to the resultant transistor. The two ends of the first wire are functionally equivalent to the collector and emitter of a conventional bipolar transistor. Both ends of the second wire are connected to the base.

The principal advantage of the molecular wire transistor is that a three-terminal device that has gain can be created using an assembly method which uses chemical properties and self-assembly, rather than requiring extreme precision in co-locating four or five objects to within a few nanometers of each other. The fabrication

of this MWT relies only on topology, i.e., the fact that anywhere two wires intersect, the device is formed. By creating such a device where one wire is doped, such as to change the electrical properties of the other wire, either NPN or PNP bipolar transistors can be formed. The type of transistor desired is formed by choosing the molecules  
5 that are applied to the surfaces of the two semiconducting wires used to form the transistor; see FIG. 4. This control can be determined by the intrinsic strength, e.g., the pKa of the Lewis acids or bases (molecular electron acceptors or donors, respectively) of the two different molecules used to coat the wires, or it can depend on the relative concentrations of the two types of molecules on the molecular wires. Thus, control is  
10 achieved as to which doping type will dominate the other when the wires cross.

FIG. 4 depicts wires 12, 14 with modulation doping from external molecular coatings 20, 22, respectively. Wire 12 is shown in plan end view, while wire 14 is shown in side elevation view. The two wires 12, 14 are composed of a semiconducting material, such as silicon, and can both be made by the same process if the device  
15 they form is a homojunction, e.g., P-Si/N-Si. It will be appreciated that heterojunctions are made by crossing different wire types, e.g., Si/Ge or semiconductor/metal. Other semiconductor materials, such as III-V and II-VI, may also be used.

In one embodiment, the wires 12, 14 are functionalized, as shown by lines 20, 22, representing functional groups. Functionalization is achieved by forming different  
20 external molecular coatings in separate processes. The nature of the coating determines the electronic properties of the wire. For example, electron withdrawing groups (Lewis acids), such as ammonia, hydrogen sulfide, amines, and sulfides, form P-type coatings 20 and electron donating groups (Lewis bases), such as boron-containing compounds (e.g.,  $\text{BF}_3$ ), form N-type coatings 22. The lengths of the tails of the molecular dopants 20, 22 will control the separation of the wires 12, 14 at their contact  
25 point.

FIG. 5 illustrates the structure of a transistor 32 of the present invention that is analogous, and functionally equivalent, to a bipolar transistor. The two ends of one wire 14 form the emitter 34a and collector 34b. Both ends of the other wire 12, being  
30 of opposite conductivity, define a very localized region 36 in first wire 14. The local-

"Field Effect" Transistors

It is also possible, in accordance with the present invention,, to have only one of the wires, say, wire 14, made of a semiconductor, and to have the other wire 12 made of a metal. This permits formation of a field effect transistor (FET) 38, in which  
5 the semiconductor wire 14 becomes the transistor and the metal wire 12 induces formation of a gate 40 in the semiconductor wire. FIG. 6 depicts this structure, which depends on the molecules that induce the gate 40 of the FET 38 creating a sufficient standoff distance from the metal wire 12 to insulate it from the gate. The gate 40 is formed between source and drain regions 42a, 42b, which, in fact, are defined by the  
10 creation of the gate in wire 14.

Examples of the metal comprising the metal wire include, but are not limited to, aluminum, silver, gold, titanium, copper, cobalt, nickel, and alloys thereof, as well as cobalt silicide, titanium silicide, and nickel silicide.

The structure of the FET 38, where both the pKa of the doping molecules and  
15 the effective standoff distance can be independently controlled, thereby permits independent control of different design parameters of the resulting FET 38. There is experimental evidence that semiconductors will form FETs at these nanometer dimensions; see, e.g., L. Guo et al, "Nanoscale silicon field effect transistors fabricated using imprint lithography", Applied Physics Letters, Vol. 71, pp. 1881-1883 (29 September 1997); L. Guo et al, "A Single-Electron Transistor Memory Operating at Room Temperature", Science, Vol. 275, pp. 649-651 (31 January 1997); and S.J. Tans et al, "Room-temperature transistor based on a single carbon nanotube", Nature, Vol. 393, pp. 49-52 (7 May 1998).

In one embodiment, as shown in FIG. 6, the portions 20a of the molecules  
25 coating the metal wire 12 are insulating and control the stand-off distance and thus the effective capacitance and field at the gate 40. The portions 20 of the molecules attached to the metal wire 12 are Lewis acid groups, and thus create, or induce, a P-type semiconducting region 40 (the gate) in the nominally N-type wire 14, which is coated with a Lewis base 22. The resulting transistor is referred to as a P-channel FET. Conversely, we could have a nominally P-type wire 14, which is coated with a Lewis acid,  
30

and a metal wire 12 provided with insulating molecular portions and Lewis base groups to form an N-channel FET of the opposite type (not shown, but the same construction, with the N- and P-types reversed). Both types (P-channel and N-channel) could be used in conjunction in much the same way as CMOS transistors are presently used.

While the foregoing description is primarily directed to providing the semiconductor wire with a Lewis acid or Lewis base coating, in fact, that wire may alternatively be a doped semiconductor wire.

10 Further Considerations

In actual construction, it is possible that a hybridization of both types of transistors, bipolar and FET, may be formed.

Further, the fabrication of bipolar transistors and FETs described above relies only on the nature of the wires 12, 14 and on the nature of the coatings 20, 22 on the wires, respectively. However, incorporating the teachings of a crossed wire switch, discussed above, which employs a bi-stable molecule at the junction of the two wires, it becomes possible to incorporate a molecular memory effect (state change) into the coatings that dope the wires. For example, by choosing the molecule that does the doping of the gate 40 to have two distinct oxidation-reduction (redox) states, a conductive state and a relatively insulating state with a large I-V hysteresis separating the two, it then becomes possible to have a special type of transistor. If the state change is set, then a transistor is created, but if the state change is not set, then either an open or closed switch exists. The open or closed condition of the switch is determined by the chemical state of the coatings on the wires - oxidized or reduced. Alternatively, a separate bi-stable molecule 16, which forms a junction at 18, could be provided, separate and distinct from the two wire coatings 20, 22. The bi-stable molecule 16 may be irreversible (singly configurable) or reversible (reconfigurable).

The state change is induced by biasing the wires with a voltage that is greater than the operating voltage of the transistor. The transistor 32, 38 typically operates in the range of about 0.5 to 1 V. The voltage inducing the state change is at least twice

this value. Alternatively, voltage of the opposite polarity may be used to induce the state change.

FIG. 7 presents an embodiment of a crossbar 44 which employs the molecular wire transistors 32, 38 of the present invention. The crossbar 44, which is disclosed and claimed in co-pending application Serial No. \_\_\_\_\_, filed on even date herewith [PD-10981966-1], consists of a layer of vertical nanowires 12 and a layer of horizontal nanowires 14. Junctions 18 are formed where the vertical wires 12 and the horizontal wires 14 cross. Distinct electrical nets (one indicated by dashed lines 46, one indicated by heavy solid lines 48, and one indicated by dotted lines 50) may be created in the crossbar 44 as part of an integrated circuit. These separate circuits 46, 48, 50 can cross each other without being electrically connected where a crossbar switch is open, denoted 52 (not conducting current). Alternatively, horizontal and vertical wires may be electrically connected by switches that are closed, denoted 54, 56, 58, 60, 62. Circuits may be confined to segments of horizontal or vertical crossbar wires by controlled oxidation of a nanowire to make an electrically open switch, denoted 64, 66, 68, 70, 72, 74, 76, 78. By using the voltage across the electrochemical cell formed by each pair of crossed nanowires to make and break electrical connections both along wires in a layer (segmented wires) and between wires in two layers (vias), one can create an integrated circuit of arbitrarily complex topology. The wires may connect to an electronic device (e.g., resonant tunneling diode or transistor) (not shown) external to the crossbar array 44. Alternatively two or more nets, e.g., 46, 48 may connect to an electronic device 80 (e.g., resonant tunneling diode or transistor) internal to the crossbar array 44. The electronic device, whether external or internal 80, may comprise a transistor 32, 38 of the present invention.

In the circuit depicted in FIG. 7, it is to be understood that all pairs of wires 12, 14 which cross will have the switch 18 between them open unless it specifically intended to be closed by the design of the integrated circuit. The freedom of a circuit designer to arbitrarily select the mixture of device types and interconnect topologies (of which FIG. 7 only shows arbitrary examples) makes the circuit valuable.

Thus, there has been disclosed molecular wire transistors, both bipolar and FETs, comprising crossed nanometer-scale wires, with two wires comprising oppositely-doped semiconductors (a bipolar transistor where the base is modulation-doped) or one wire comprising a doped semiconductor and the other a coated metal wire (an 5 FET where the gate is modulation-doped). In either case, both wires are joined by functionalized groups at the intersecting junctions. It will be apparent to those skilled in this art that various changes and modifications of an obvious nature may be made, and all such changes and modifications are considered to fall within the scope of the appended claims.

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U.S. PATENT AND TRADEMARK OFFICE

CLAIMSWhat Is Claimed Is:

- 5        1. A molecular wire transistor comprising a pair of crossed wires, at least one of said wires comprising a doped semiconductor material, said pair of crossed wires forming a junction where one wire crosses another, a first semiconductor wire being of a first conductivity type and a second wire being provided with either Lewis acid functional groups or Lewis base functional groups to create a region of modulation doping of a second and opposite conductivity type in said junction.
- 10
- 15        2. The molecular wire transistor of Claim 1 wherein one of said wires comprises a semiconductor material and is nanoscopic in the direction of the shortest line between the two wires.
- 20        3. The molecular wire transistor of Claim 2 wherein the other wire is nanoscopic or larger in the direction of the shortest line between the two wires.
- 25        4. The molecular wire transistor of Claim 1 wherein one of said wires comprises N-doped semiconductor and the other wire comprises P-doped semiconductor.
5. The molecular wire transistor of Claim 4 wherein one wire of a given doping comprises emitter and collector regions and the other wire, being of the opposite doping, induces a base region by modulation doping on said wire containing said emitter and collector regions at said junction where said wires cross, said base region formed between said emitter and collector portions.
6. The molecular wire transistor of Claim 5 wherein a PNP bipolar transistor is formed.

7. The molecular wire transistor of Claim 5 wherein an NPN bipolar transistor is formed.

8. The molecular wire transistor of Claim 1 wherein one of said wires comprises  
5 doped semiconductor and the other wire comprises a metal.

9. The molecular wire transistor of Claim 8 wherein said doped semiconductor  
wire comprises source and drain regions and said metal wire inducing said gate by  
modulation doping on said doped semiconductor wire where said wires cross, between  
10 said source and drain regions, said functional groups on said metal wire comprising a  
first portion extending from said metal wire being electrically insulating and a second  
portion joined to said first portion comprising said Lewis acid or base functional group.

10. The molecular wire transistor of Claim 9 wherein an N-channel field effect  
15 transistor is formed.

11. The molecular wire transistor of Claim 9 wherein a P-channel field effect  
transistor is formed.

20 12. The molecular wire transistor of Claim 1 wherein both said semiconductor  
wires are provided with functional groups, one said wire being provided with Lewis acid  
functional groups and the other said wire being provided with Lewis base functional  
groups.

25 13. The molecular wire transistor of Claim 1 wherein either said Lewis acid  
functional groups or said Lewis base functional groups have two distinct oxidation-  
reduction states, a conductive state and a relatively insulating state with a large I-V  
hysteresis separating the two states, to form a state change transistor or a switch that is  
30 capable of being set by application of a voltage that is larger than the voltage at which  
the transistor operates.

14. The molecular wire transistor of Claim 13 wherein said state change is set, thereby forming a transistor.

5        15. The molecular wire transistor of Claim 13 wherein said state change is not set, thereby forming either an open or closed switch.

10      16. A method for fabricating a molecular wire transistor comprising a pair of crossed wires, at least one of said wires comprising a doped semiconductor material, said method comprising providing a first said wire having a first conductivity type, providing a second said wire with either Lewis acid functional groups or Lewis base functional groups to provide said second wire with a second conductivity type opposite to that of said first wire, and causing said pair of wires to cross, thereby forming a junction with modulation doping where one wire crosses another.

15

17. The method of Claim 16 wherein one of said wires comprises a semiconductor material and is nanoscopic in the direction of the shortest line between the two wires.

20

18. The method of Claim 17 wherein the other wire is nanoscopic or larger in the direction of the shortest line between the two wires.

19. The method of Claim 16 wherein one of said wires comprises N-doped semiconductor and the other wire comprises P-doped semiconductor.

25

20. The method of Claim 19 wherein one wire of a given doping induces a base region by modulation doping in said other wire around said junction, thereby defining emitter and collector regions on either side of said base region in said other wire.

30

21. The method of Claim 20 wherein a PNP bipolar transistor is formed.

22. The method of Claim 20 wherein an NPN bipolar transistor is formed.
23. The method of Claim 16 wherein one of said wires comprises doped semi-conductor and the other wire comprises a metal.  
5
24. The method of Claim 23 wherein said functional groups on said metal wire comprise a first portion that is electrically insulating and extends from said metal wire and a second portion joined to said first portion comprising said Lewis acid or base functional group and wherein said metal wire induces a gate region in said doped semiconductor wire around said junction, thereby defining source and drain regions on either side of said gate region in said other wire.  
10
25. The method of Claim 24 wherein an N-channel field effect transistor is formed.  
15
26. The method of Claim 24 wherein a P-channel field effect transistor is formed.
- 20 27. The method of Claim 16 wherein both said semiconductor wires are provided with functional groups, one said wire being provided with Lewis acid functional groups and the other said wire being provided with Lewis base functional groups.
- 25 28. The method of Claim 16 wherein either said Lewis acid functional groups or said Lewis base functional groups have two distinct oxidation-reduction states, a conductive state and a relatively insulating state with a large I-V hysteresis separating the two states, to form a state change transistor or a switch that is capable of being set by application of a voltage that is larger than the voltage at which the transistor operates.  
30

29. The method of Claim 28 wherein said state change is set, thereby forming a transistor.

30. The method of Claim 28 wherein said state change is not set, thereby  
5 forming either an open or closed switch.

31. A crossbar array of crossed-wire devices, each device comprising a junction formed by a pair of crossed wires where one wire crosses another, said junction having a functional dimension in nanometers, wherein at least one said junction in  
10 said crossbar array comprises a molecular wire transistor comprising a pair of crossed wires, at least one of said wires comprising a doped semiconductor material, said pair of crossed wires forming a junction where one wire crosses another, a first semiconductor wire being of a first conductivity type and a second wire being provided with either Lewis acid functional groups or Lewis base functional groups to create a region of  
15 modulation doping of a second and opposite conductivity type in said junction.

32. The crossbar array of Claim 31 wherein one of said wires comprises a semiconductor material and is nanoscopic in the direction of the shortest line between the two wires.

20  
33. The crossbar array of Claim 32 wherein the other wire is nanoscopic or larger in the direction of the shortest line between the two wires.

34. The crossbar array of Claim 31 wherein one of said wires comprises N-doped semiconductor and the other wire comprises P-doped semiconductor.  
25

35. The crossbar array of Claim 34 wherein one wire of a given doping comprises emitter and collector regions and the other wire, being of the opposite doping, induces a base region by modulation doping on said wire containing said emitter and col-

lector regions at said junction where said wires cross, said base region formed between said emitter and collector portions.

36. The crossbar array of Claim 35 wherein a PNP bipolar transistor is formed.

5

37. The crossbar array of Claim 35 wherein an NPN bipolar transistor is formed.

38. The crossbar array of Claim 31 wherein one of said wires comprises doped semiconductor and the other wire comprises a metal.

10

39. The crossbar array of Claim 38 wherein said doped semiconductor wire comprises source and drain regions and said metal wire inducing said gate by modulation doping on said doped semiconductor wire where said wires cross, between said source and drain regions, said functional groups on said metal wire comprising a first portion extending from said metal wire being electrically insulating and a second portion joined to said first portion comprising said Lewis acid or base functional group.

15  
40. The crossbar array of Claim 39 wherein an N-channel field effect transistor is formed.

20

41. The crossbar array of Claim 39 wherein a P-channel field effect transistor is formed.

25

42. The crossbar array of Claim 31 wherein both said semiconductor wires are provided with functional groups, one said wire being provided with Lewis acid functional groups and the other said wire being provided with Lewis base functional groups.

30

43. The crossbar array of Claim 31 wherein either said Lewis acid functional groups or said Lewis base functional groups have two distinct oxidation-reduction states, a conductive state and a relatively insulating state with a large I-V hysteresis

separating the two states, to form a state change transistor or a switch that is capable of being set by application of a voltage that is larger than the voltage at which the transistor operates.

5        44. The crossbar array of Claim 43 wherein said state change is set, thereby forming a transistor.

45. The crossbar array of Claim 43 wherein said state change is not set, thereby forming either an open or closed switch.

10      46. The crossbar array of Claim 31 further including at least one connector species connecting said pair of crossed wires.

## MOLECULAR WIRE TRANSISTOR (MWT)

ABSTRACT OF THE DISCLOSURE

5       Bipolar and field effect molecular wire transistors are provided. The molecular  
wire transistor comprises a pair of crossed wires, with at least one of the wires comprising  
a doped semiconductor material. The pair of crossed wires forms a junction  
where one wire crosses another, one wire being provided with Lewis acid functional  
groups and the other wire being provided with Lewis base functional groups. If both  
10      wires are doped semiconductor, such as silicon, one is P-doped and the other is N-  
doped. One wire of a given doping comprises the emitter and collector portions and  
the other wire comprises the base portion, which is formed by modulation doping on  
the wire containing the emitter and collector at the junction where the wires cross and  
between the emitter and collector portions, thereby forming a bipolar transistor. Both  
15      NPN and PNP bipolar transistors may be formed. Analogously, one wire may comprise  
doped semiconductor, such as silicon, and the other wire a metal, the doped silicon  
wire forming the source and drain and the metal wire forming the gate by modulation  
doping on the doped silicon wire where the wires cross, between the source and drain, to  
form a field effect transistor. Both P-channel and N-channel FETs may be formed. The  
20      construction of both bipolar transistors and FETs on a nanometer scale, which are  
self-aligned and modulation-doped, is thereby enabled.

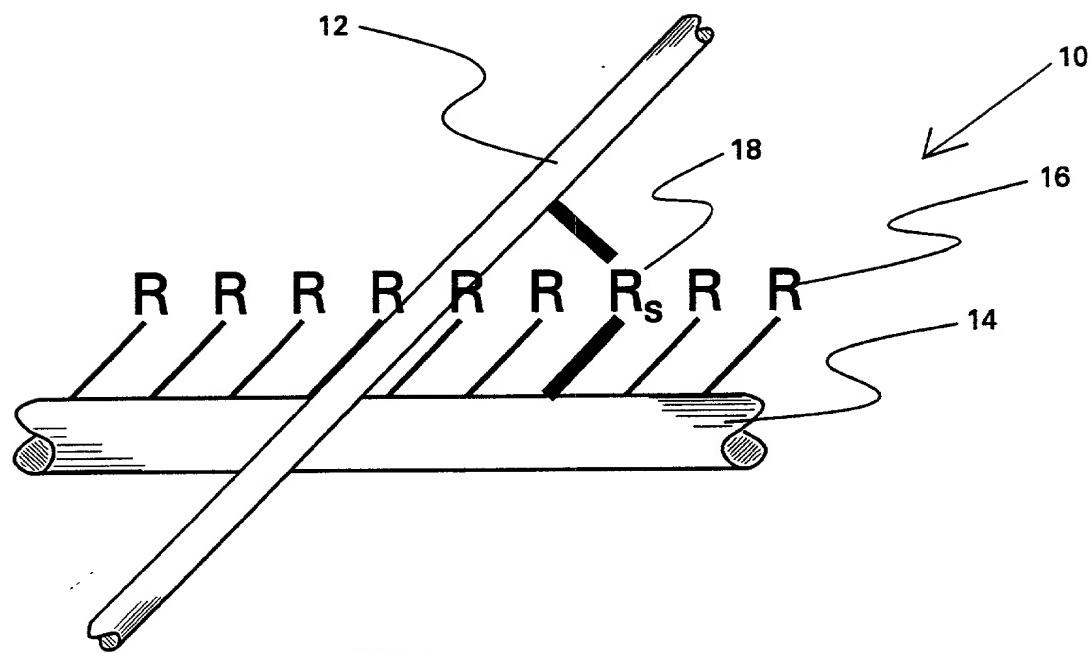


FIG. 1a

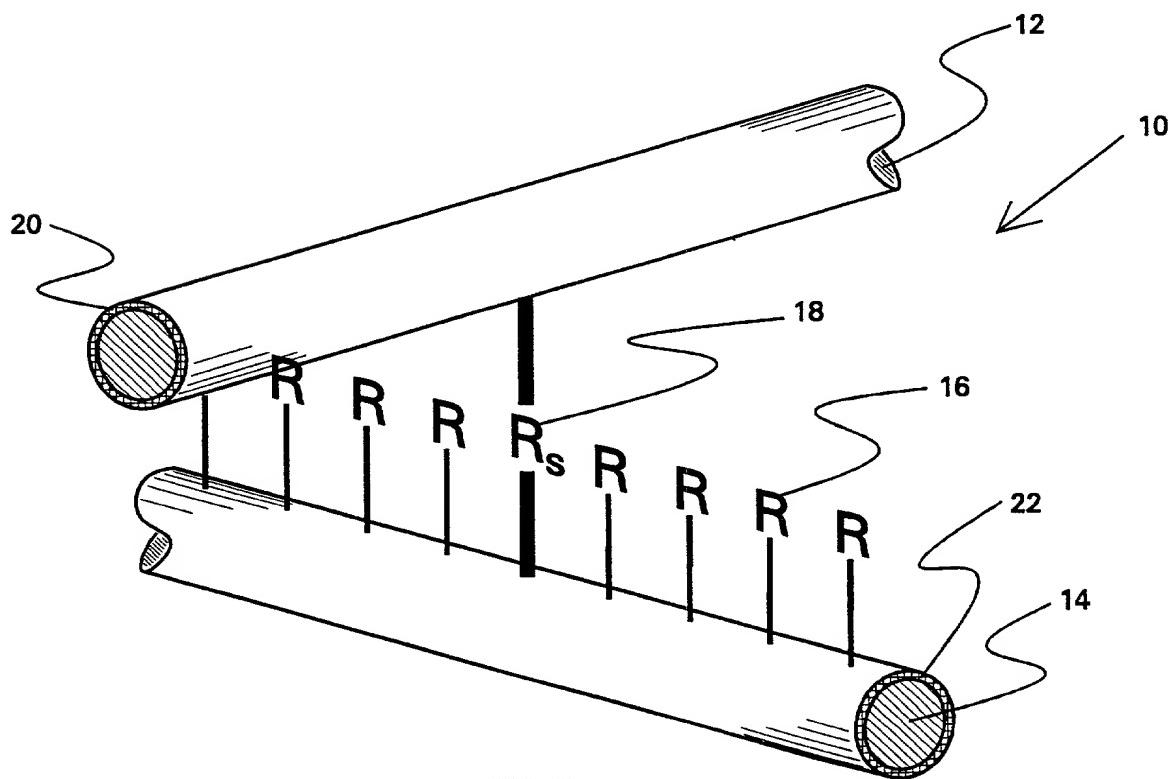
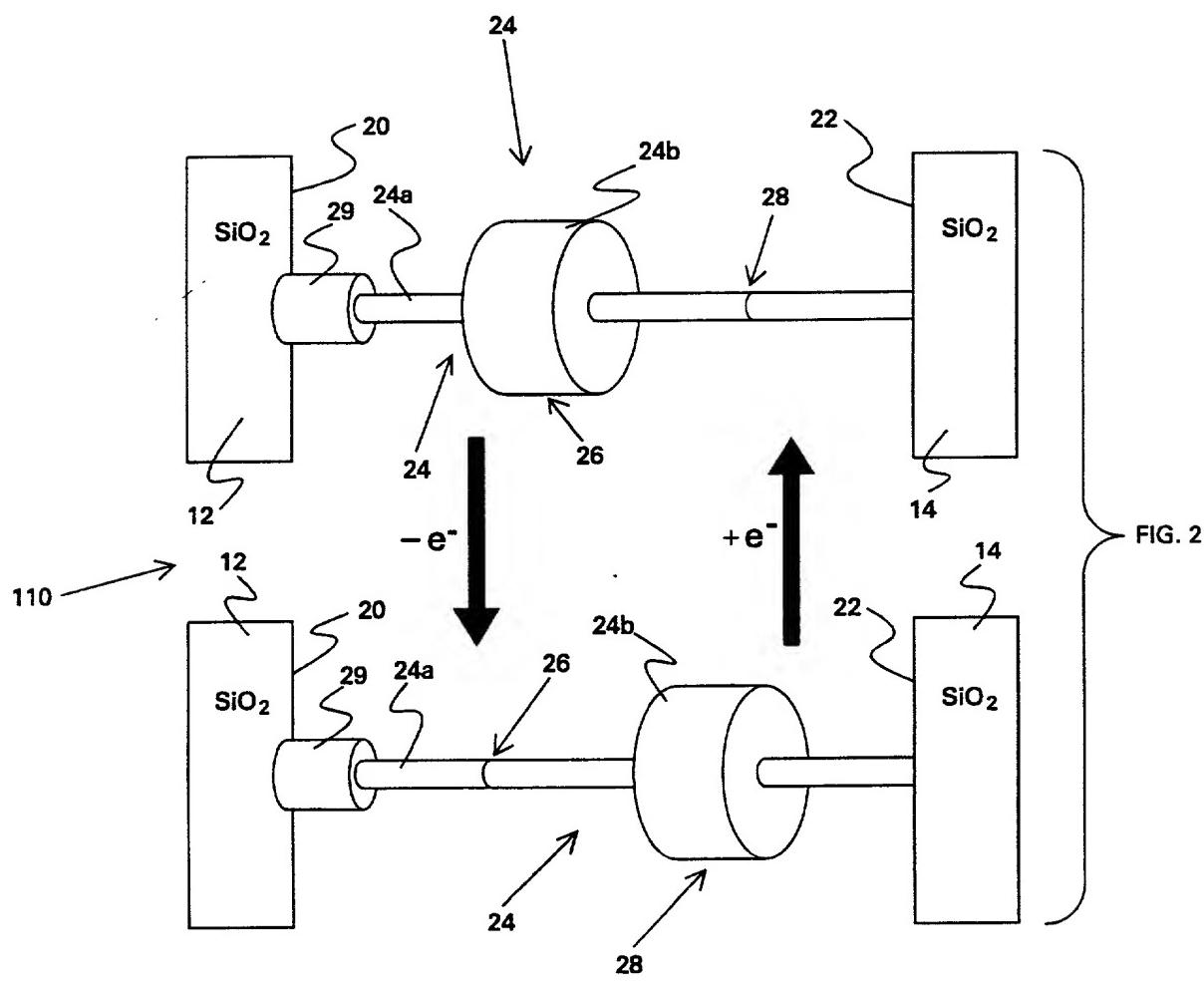
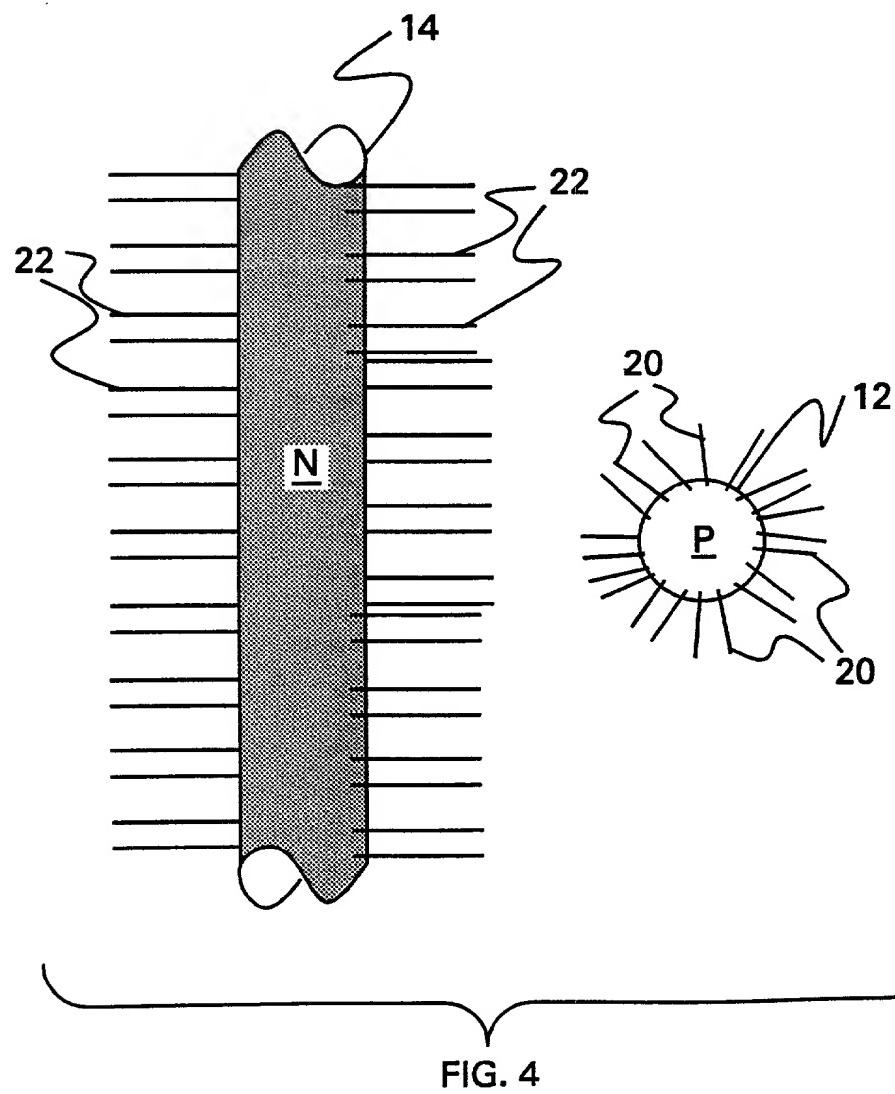
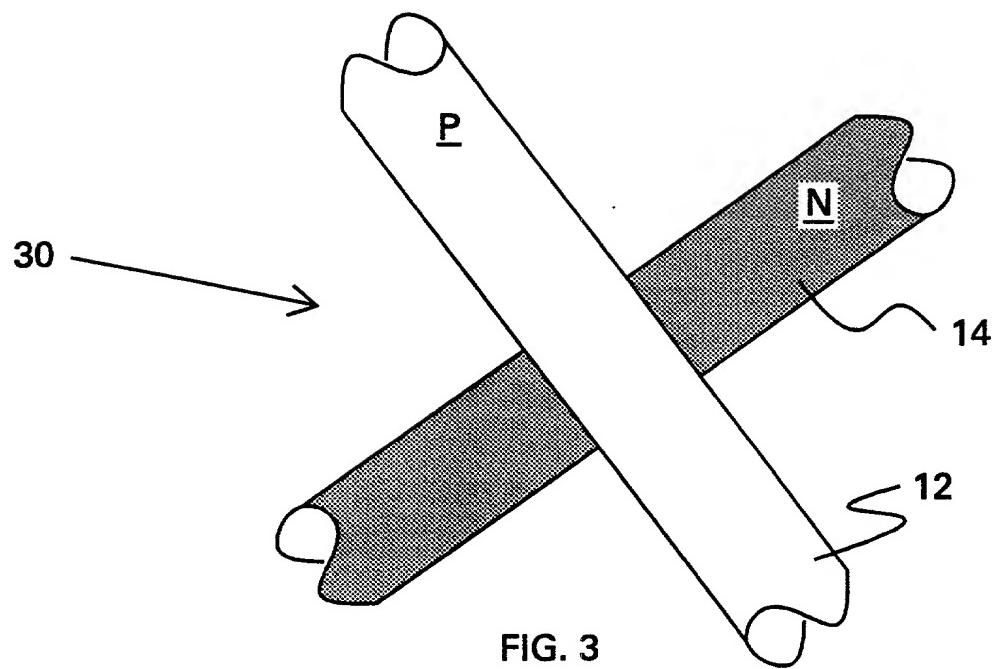


FIG. 1b





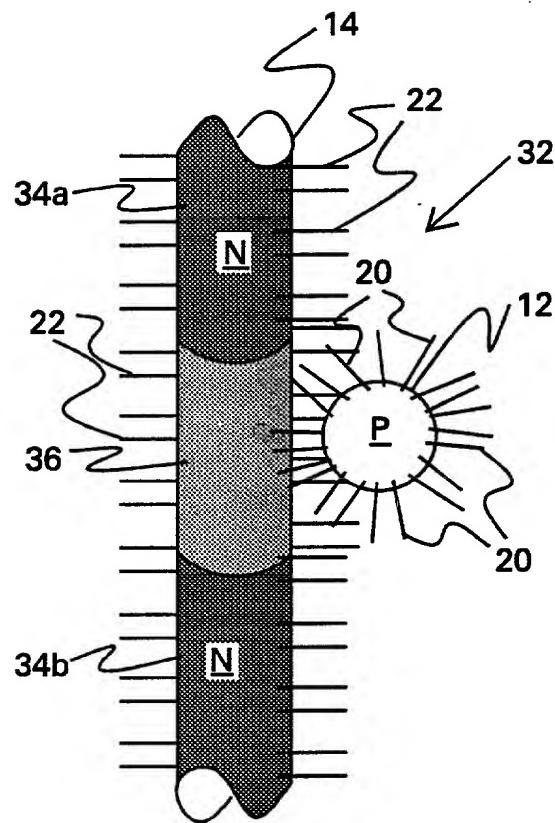


FIG. 5

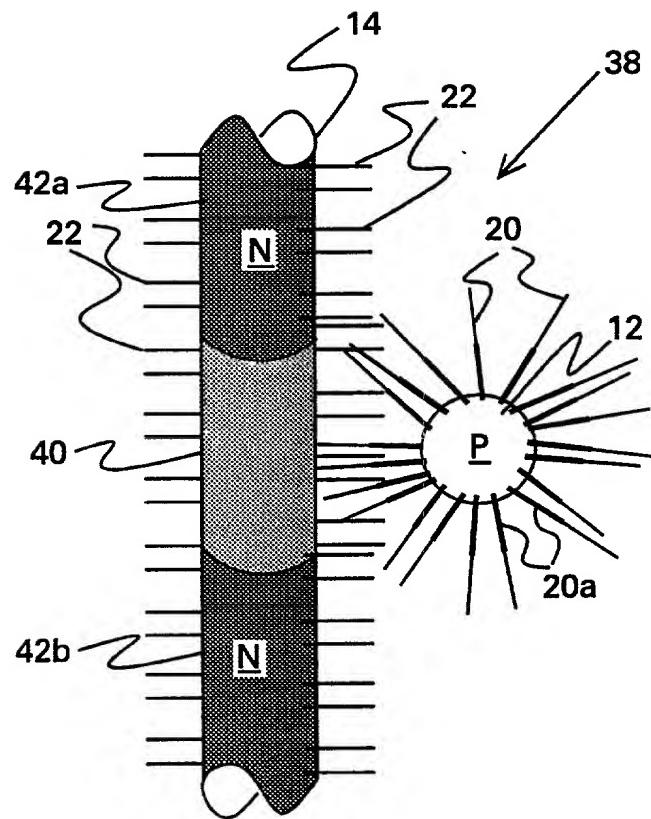


FIG. 6

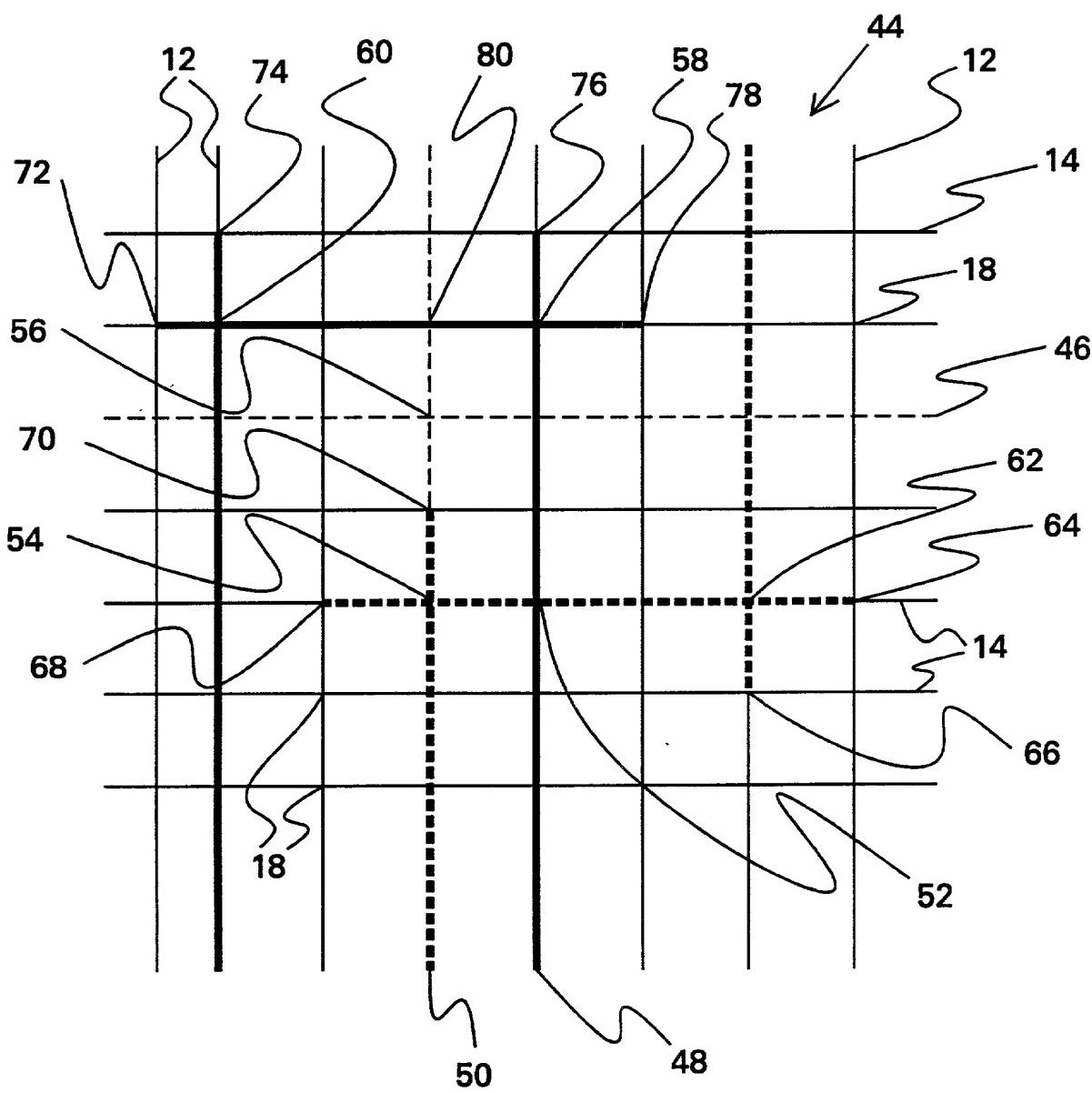


FIG. 7

**DECLARATION AND POWER OF ATTORNEY  
FOR PATENT APPLICATION**

ATTORNEY DOCKET NO. 10981967

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**MOLECULAR WIRE TRANSISTOR (MWI)**

the specification of which is attached hereto unless the following box is checked:

( ) was filed on \_\_\_\_\_ as US Application Serial No. or PCT International Application Number \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

**Foreign Application(s) and/or Claim of Foreign Priority**

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

| COUNTRY | APPLICATION NUMBER | DATE FILED | PRIORITY CLAIMED UNDER 35 U.S.C. 119 |
|---------|--------------------|------------|--------------------------------------|
|         |                    |            | YES: _____ NO: _____                 |
|         |                    |            | YES: _____ NO: _____                 |

**Provisional Application**

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

| APPLICATION SERIAL NUMBER | FILING DATE |
|---------------------------|-------------|
|                           |             |
|                           |             |

**U. S. Priority Claim**

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

| APPLICATION SERIAL NUMBER | FILING DATE | STATUS (patented/pending/abandoned). |
|---------------------------|-------------|--------------------------------------|
|                           |             |                                      |
|                           |             |                                      |
|                           |             |                                      |
|                           |             |                                      |

**POWER OF ATTORNEY:**

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) listed below to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Marc R. Mayer

Herbert R. Schulze

Ian Hardcastle

Reg. No. 36,211

Reg. No. 30,682

Reg. No. 34,075

|  |  |
|--|--|
| <b>Send Correspondence to:</b><br>IP Administration<br>Legal Department, 20BN<br>HEWLETT-PACKARD COMPANY<br>P.O. Box 10301<br>Palo Alto, California 94303-0890 | <b>Direct Telephone Calls To:</b><br>Marc R. Mayer<br>(650) 857-6545 |
|--|--|

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Residence: Menlo Park, California 94025

Post Office Address: Same as Residence

3-2-99

Inventor's Signature

Date

**DECLARATION AND POWER OF ATTORNEY  
FOR PATENT APPLICATION (continued)**

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Residence: Mountain View, California 94040

Post Office Address: Same as Residence

Inventor's Signature: R. Stanley Williams

Date: March 2, 1999

Full Name of # 3 joint inventor: \_\_\_\_\_ Citizenship: \_\_\_\_\_

Residence: \_\_\_\_\_

Post Office Address: \_\_\_\_\_

Inventor's Signature: \_\_\_\_\_ Date: \_\_\_\_\_

Full Name of # 4 joint inventor: \_\_\_\_\_ Citizenship: \_\_\_\_\_

Residence: \_\_\_\_\_

Post Office Address: \_\_\_\_\_

Inventor's Signature: \_\_\_\_\_ Date: \_\_\_\_\_

Full Name of # 5 joint inventor: \_\_\_\_\_ Citizenship: \_\_\_\_\_

Residence: \_\_\_\_\_

Post Office Address: \_\_\_\_\_

Inventor's Signature: \_\_\_\_\_ Date: \_\_\_\_\_

Full Name of # 6 joint inventor: \_\_\_\_\_ Citizenship: \_\_\_\_\_

Residence: \_\_\_\_\_

Post Office Address: \_\_\_\_\_

Inventor's Signature: \_\_\_\_\_ Date: \_\_\_\_\_

Full Name of # 7 joint inventor: \_\_\_\_\_ Citizenship: \_\_\_\_\_

Residence: \_\_\_\_\_

Post Office Address: \_\_\_\_\_

Inventor's Signature: \_\_\_\_\_ Date: \_\_\_\_\_

Full Name of # 8 joint inventor: \_\_\_\_\_ Citizenship: \_\_\_\_\_

Residence: \_\_\_\_\_

Post Office Address: \_\_\_\_\_

Inventor's Signature: \_\_\_\_\_ Date: \_\_\_\_\_